STM32L4xx Technical Training

MCD Application Team

15W05 Prague

STM32 L4

life.augmented

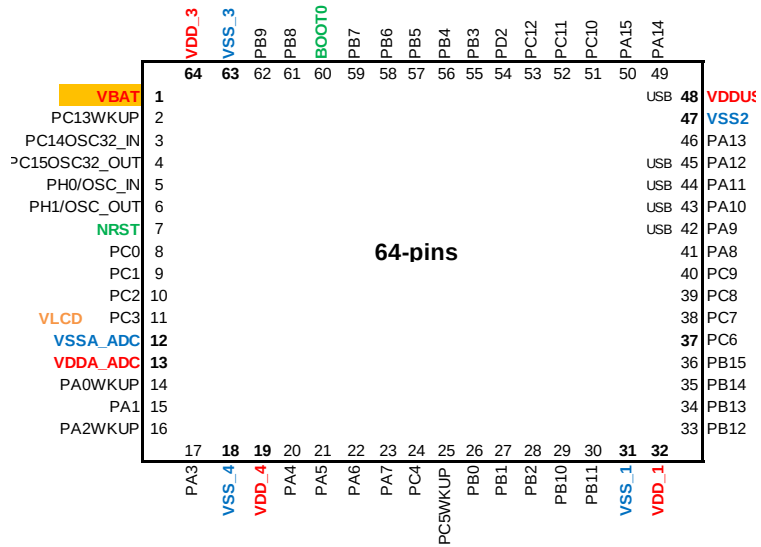
Families migration to STM32L4

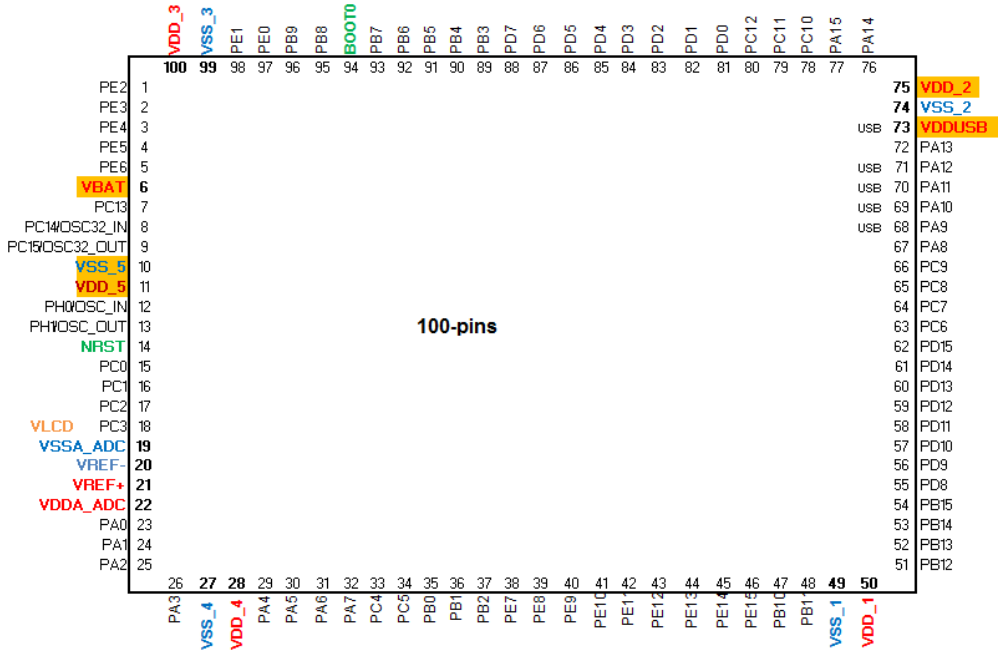
life.augmented

ARM

STM32L0 to STM32L4

- Easy transition from STM32L0 to STM32L4 :
  - VLCD is replaced by VBAT (VLCD is now multiplexed with PC3)
  - PH9/PH10 replaced by VSS/VDD
  - Pin 73 and 75 are swapped (VDD / VDDUSB)
  - Pins functions mapping near 100% compatible for common features

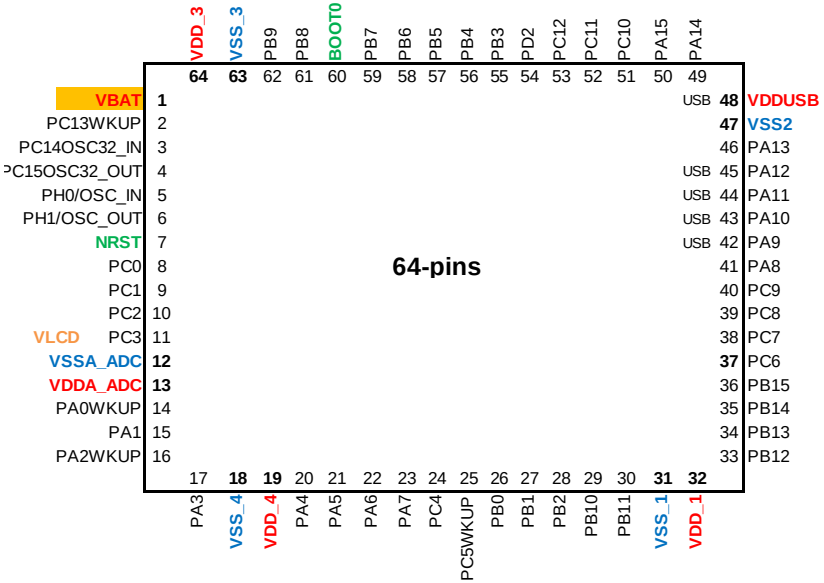


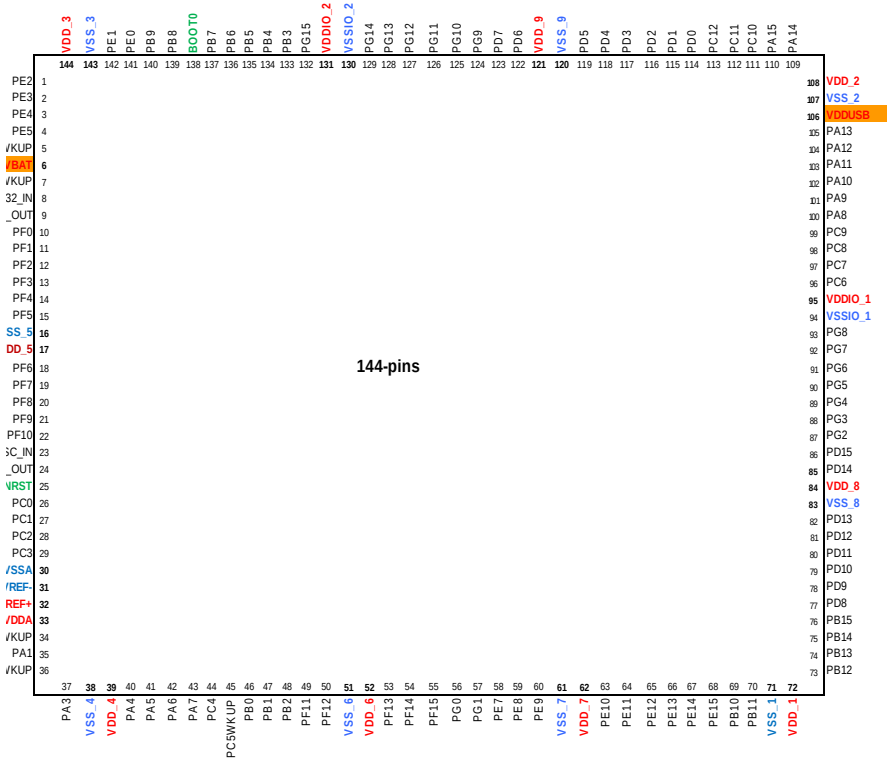


life.augmented

STM32L1 to STM32L4

- Easy transition from STM32L1 to STM32L4 :
  - VLCD is replaced by VBAT (VLCD is now multiplexed with PC3)
  - 144/100 pin : PH2 replaced by VDDUSB (USB dedicated supply)
  - Pins functions mapping near 100% compatible for common features



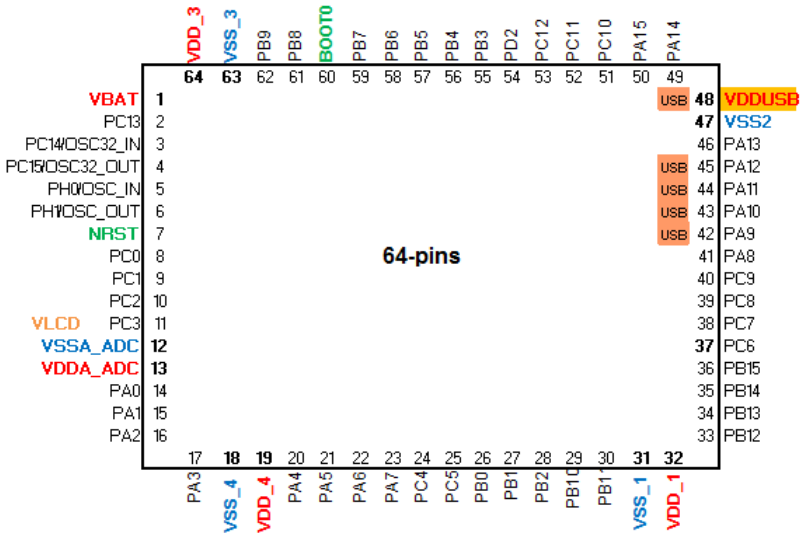


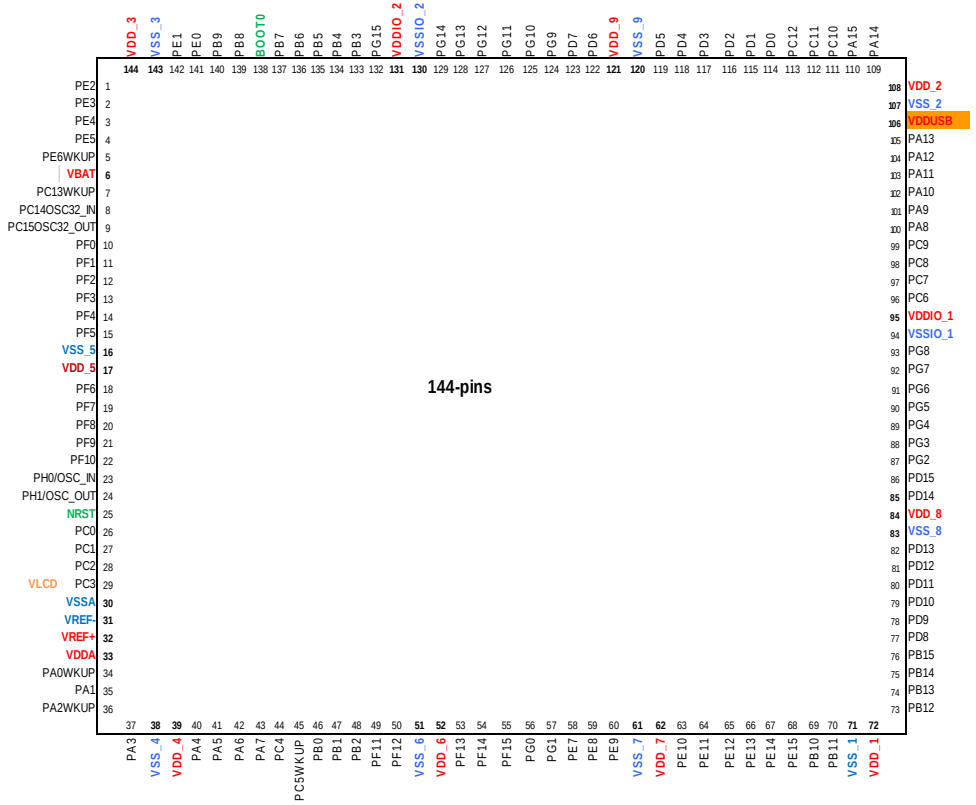
Please refer to **AN4612** for more details on STM32L1 to STM32L4 migration

life.augmented

STM32F1 to STM32L4

- Easy transition from STM32F1 to STM32L4 :
  - 144/100 pin : non connected pin replaced by VDDUSB (USB dedicated supply).
  - 64 pin : VDD replaced by VDDUSB (USB dedicated supply)
  - Pins functions mapping near 100% compatible for common features

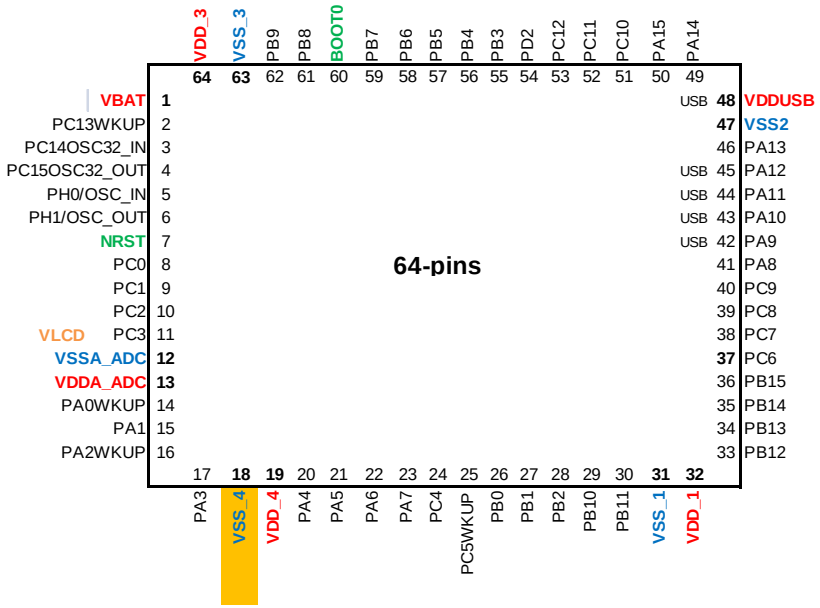


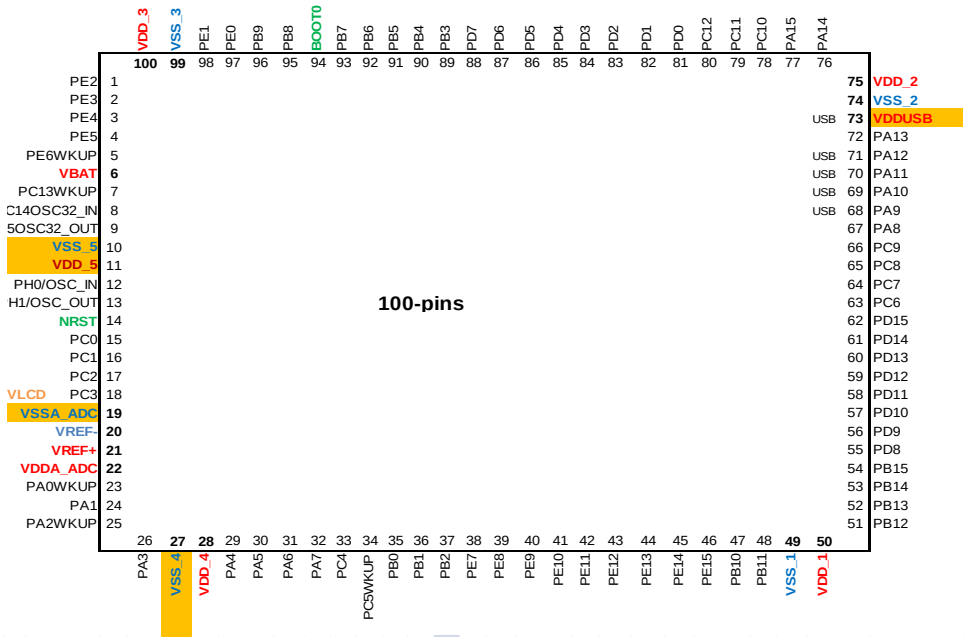


life.augmented

STM32F3 to STM32L4

- Transition from STM32F3 to STM32L4 :
  - Up to 5 GPIOs are changed into supply pins
  - Pin function mapping : high compatibility for common features but :
  - OPAMP, COMP, Touch sense mapping not compatible
  - Some remap options differ

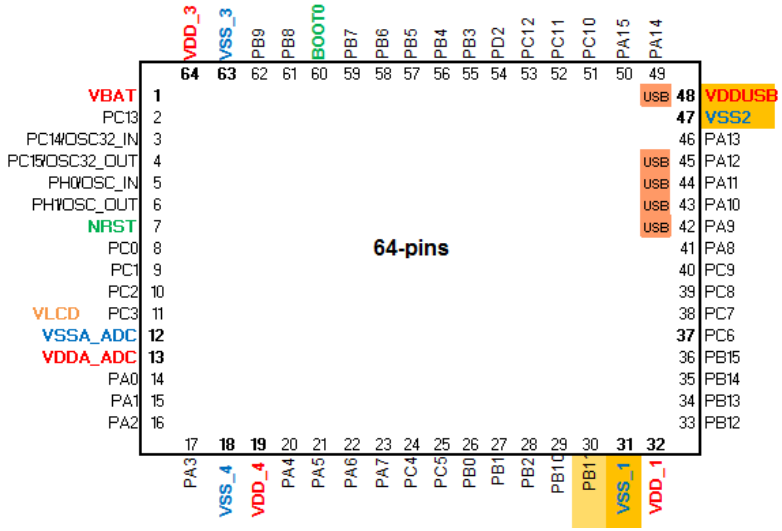


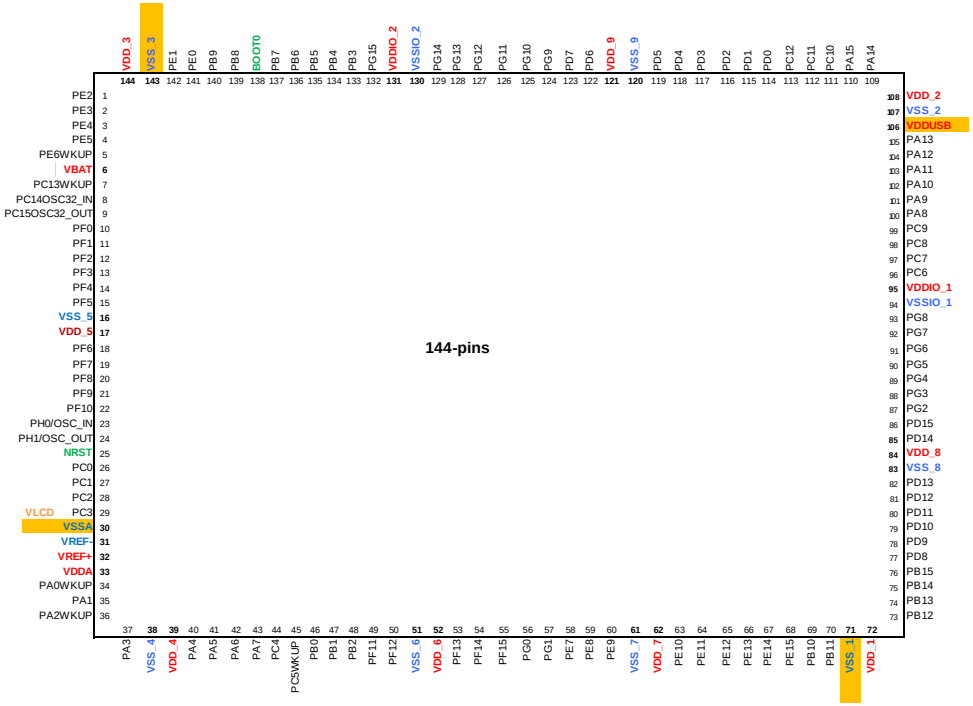


life.augmented

STM32F2/STM32F4 to STM32L4

- Transition from STM32F4 to STM32L4 :
  - Pin VDD is replaced by VSSA, PDR_ON replaced by VSS
  - VCAP1 is replaced by VSS (or PB11 on STM32F401/411 QFP64/100)
  - VCAP2 is replaced by VDDUSB (USB dedicated supply) or VSS
  - Pins functions mapping near 100% compatible for common features





Please refer to **AN4616** for more details on STM32F4 to STM32L4 migration

life.augmented

ARM Cortex M4 in few words

life.augmented

ARM

Cortex-M processors

- **Forget traditional 8/16/32-bit classifications**
  - Seamless architecture across all applications
  - Every product optimized for ultra low power and ease of use

Cortex-M0 & M0+	Cortex-M3	Cortex-M4
“8/16-bit” applications	“16/32-bit” applications	“32-bit/DSC” applications

Binary and tool compatible

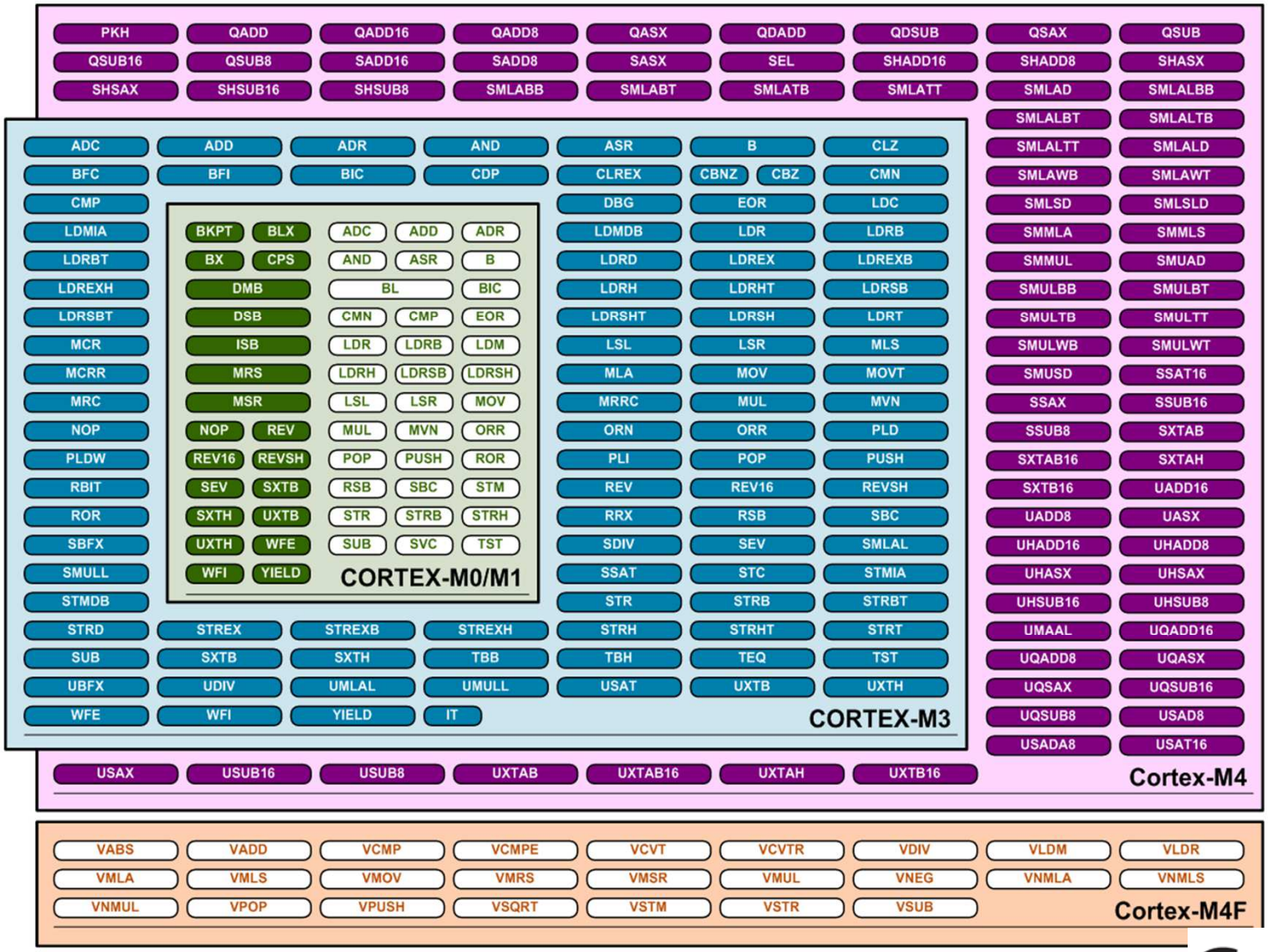








Cortex-M processors binary compatible



life.augmented

Cortex

Low-Power Leadership from ARM

ARM Cortex M4 Core

ARM

Cortex
Low-Power Leadership from ARM

FPU

Single precision
Ease of use
Better code efficiency
Faster time to market
Eliminate scaling and saturation
Easier support for meta-language tools

What is Cortex-M4?

MCU

Ease of use of C programming
Interrupt handling
Ultra-low power

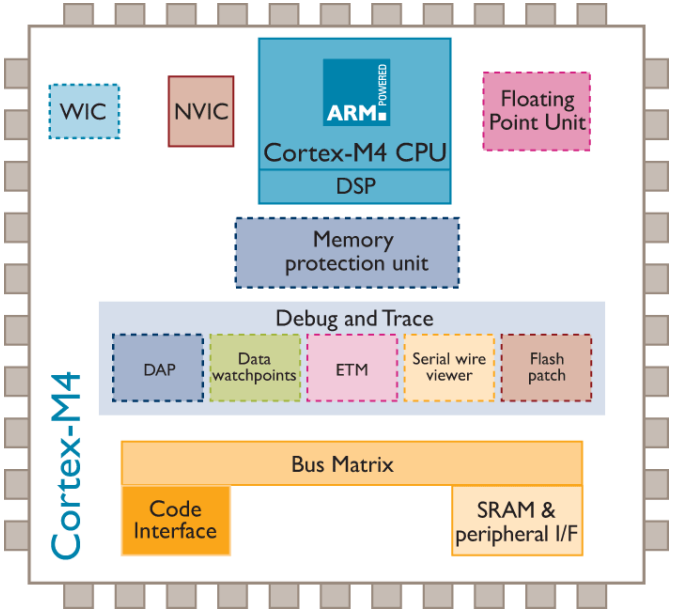
DSP

Harvard architecture
Single-cycle MAC
Barrel shifter

life.augmented

Cortex-M4 processor microarchitecure

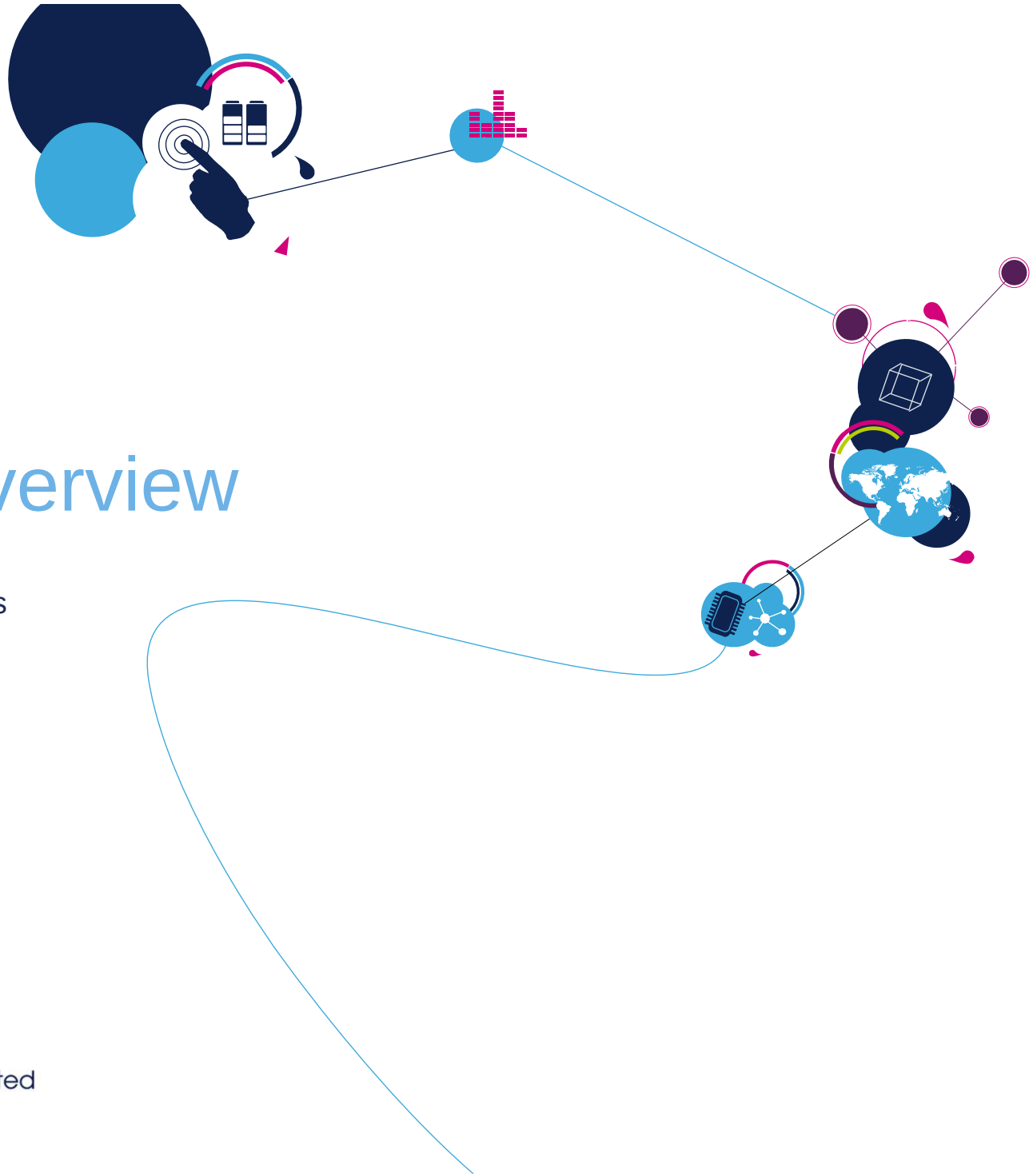
- **ARMv7ME Architecture**
  - Thumb-2 Technology
  - DSP and SIMD extensions
  - Single cycle MAC (Up to 32 x 32 + 64 -> 64)
  - Optional single precision FPU
  - Integrated configurable NVIC
  - Compatible with Cortex-M3
- **Microarchitecture**
  - 3-stage pipeline with branch speculation
  - 3x AHB-Lite Bus Interfaces
- **Configurable for ultra low power**
  - Deep Sleep Mode, Wakeup Interrupt Controller
  - Power down features for Floating Point Unit
- **Flexible configurations for wider applicability**
  - Configurable Interrupt Controller (1-240 Interrupts and Priorities)
  - Optional Memory Protection Unit
  - Optional Debug & Trace



Low-Power Leadership from ARM

Cortex-M feature set comparison

	Cortex-M0+	Cortex-M3	Cortex-M4
Architecture Version	V6M	v7M	v7ME
Instruction set architecture	Thumb, Thumb-2 System Instructions	Thumb + Thumb-2	Thumb + Thumb-2, DSP, SIMD, FP
DMIPS/MHz	0.95	1.25	1.25
Bus interfaces	1+I/O port	3	3
Integrated NVIC	Yes	Yes	Yes
Number interrupts	1-32 + NMI	1-240 + NMI	1-240 + NMI
Interrupt priorities	4	8-256	8-256
Breakpoints, Watchpoints	4/2/0, 2/1/0	8/4/0, 2/1/0	8/4/0, 2/1/0
Memory Protection Unit (MPU)	Yes (Option)	Yes (Option)	Yes (Option)
Integrated trace option (ETM)	MTB (Option)	Yes (Option)	Yes (Option)
Fault Robust Interface	No	Yes (Option)	No
Single Cycle Multiply	Yes (Option)	Yes	Yes
Hardware Divide	No	Yes	Yes
WIC Support	Yes	Yes	Yes
Bit banding support	No	Yes	Yes
Single cycle DSP/SIMD	No	No	**Yes**
Floating point hardware	No	No	**Yes**
Bus protocol	AHB Lite, I/O	AHB Lite	AHB Lite
CMSIS Support	Yes	Yes	Yes

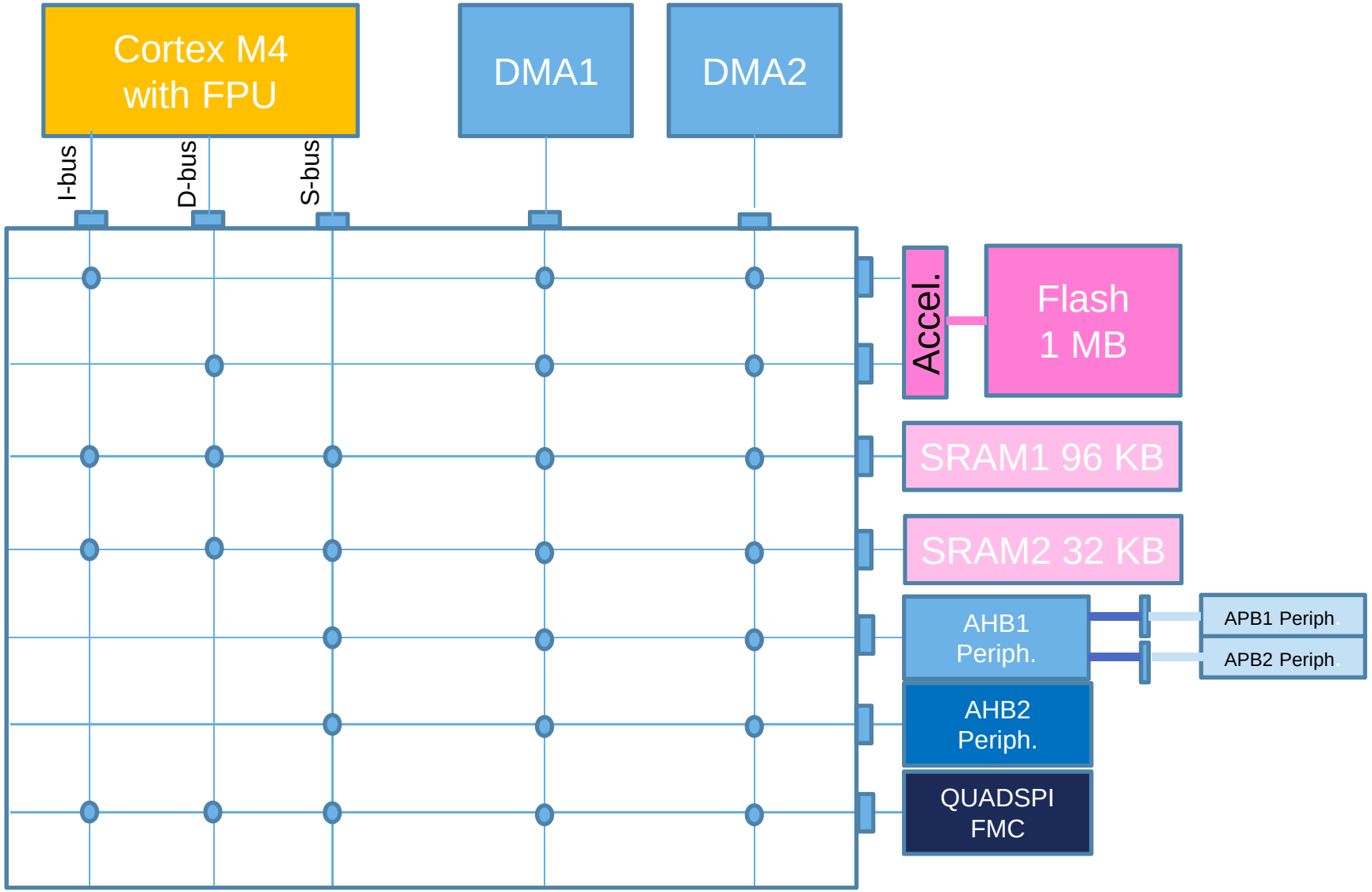


System overview

MCU Division Applications

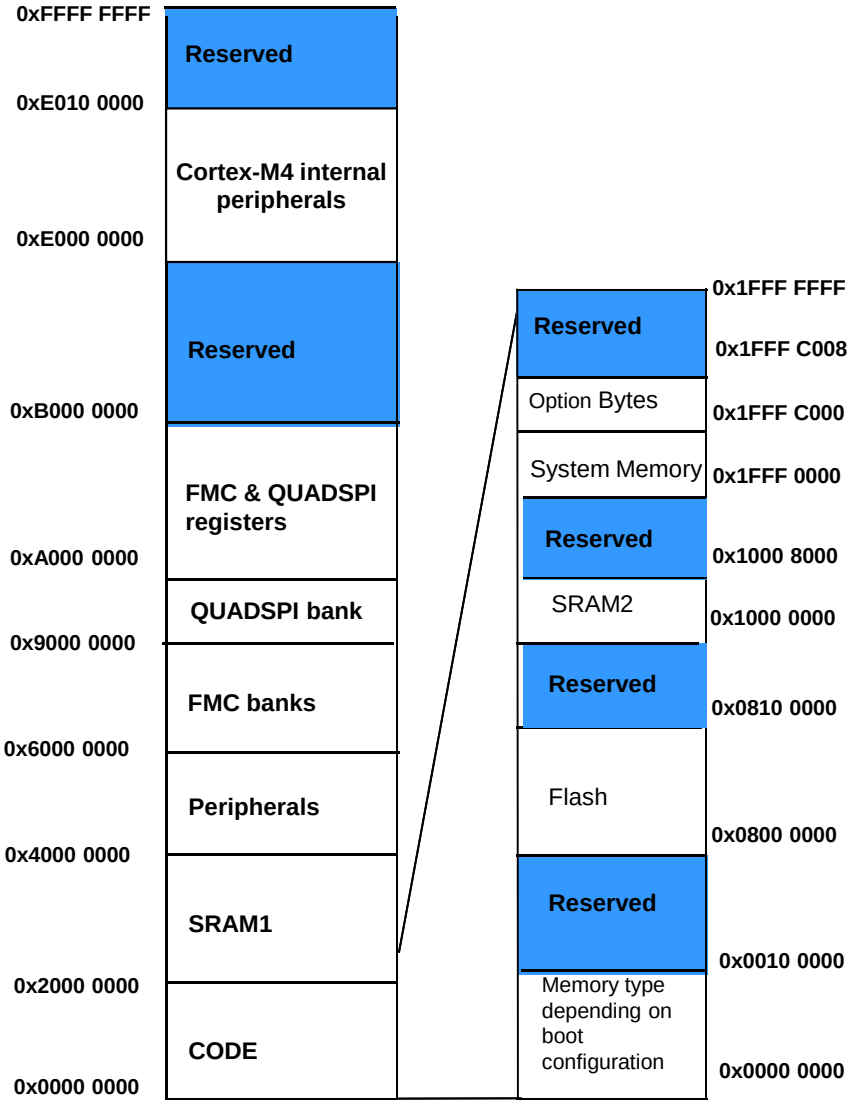
life.augmented

Bus matrix



AHB2 peripherals: GPIO, ADC, OTG_FS, AES, RNG

Memory Mapping



- **FLASH : up to 1 Mbytes, dual bank**
  - FB_MODE = 0 in SYSCFG_MEMRMP:
    - **Bank 1 @ 0x0800 0000**
    - **Bank 2 @ 0x0808 0000**
  - FB_MODE = 1 in SYSCFG_MEMRMP
    - **Bank 2 @ 0x0800 0000**
    - **Bank 1 @ 0x0808 0000**
- **SRAM: Up to 128 Kbytes SRAM split in 2 parts :**
  - SRAM1 : 96 KBytes @2000 0000
  - SRAM2 : 32 KBytes @1000 0000 :
    - Access through D-code and I-code
- **Physical remap at 0x0000 0000 selected by MEM_MODE in SYSCFG_MEMRMP:**
  - Flash Bank 1 or Bank 2 (see FB_MODE)
  - System flash
  - FMC bank 1
  - SRAM1
  - QUADSPI

life.augmented

Boot modes

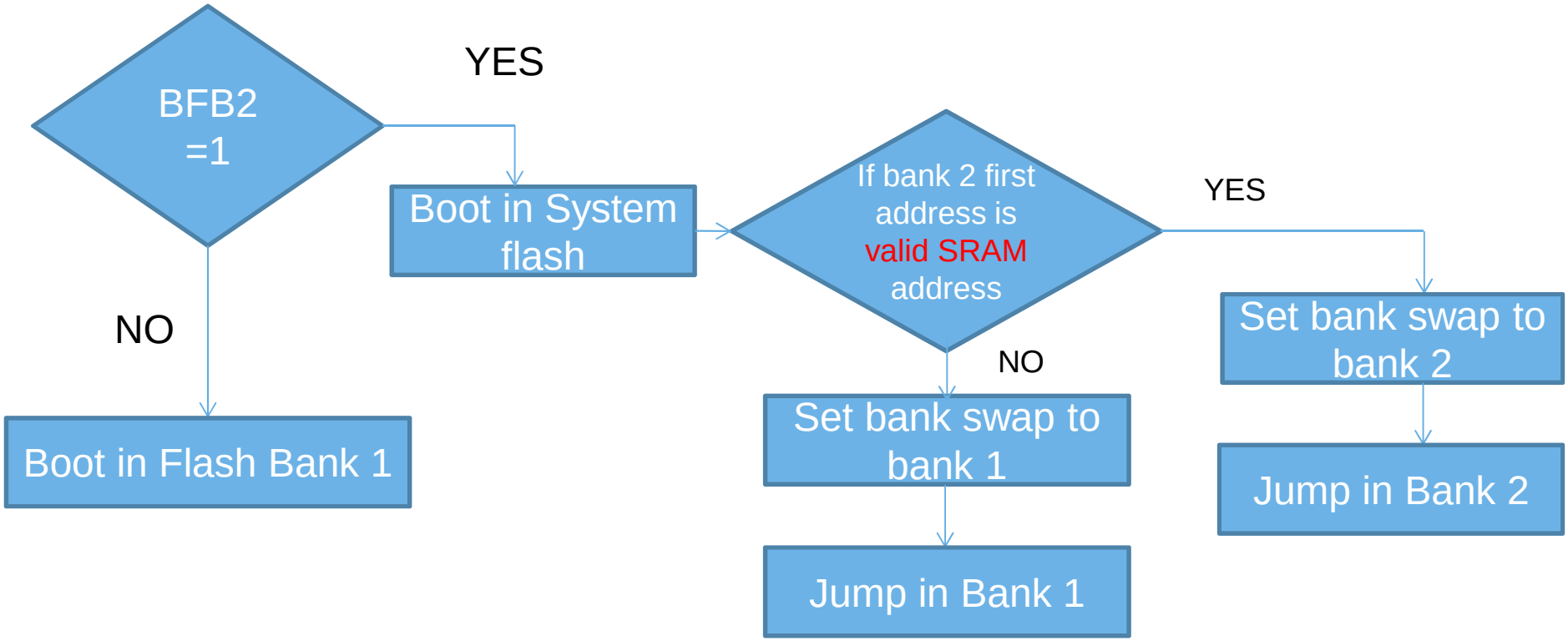
Boot mode selection		Boot mode	Aliasing
BOOT1 (opposite of nBOOT1 option bit)	**BOOT0 (pin)**		
x	0	User Flash	Main Flash memory is selected as boot space
1	1	System memory	System memory is selected as boot space
0	1	SRAM1	Embedded SRAM1 is selected as boot space

- When Boot mode = User Flash and option Bit BFB2 = 0
  - Boot is done in Flash Bank 1
- When Boot mode = User Flash and option Bit BFB2 = 1
  - Boot is done in Flash Bank 2.

Boot modes

- Dual bank boot is managed by the bootloader.

Boot 0 = 0 : Boot mode = Flash



Bootloader is intrusive in SRAM area 0x2000 0000 - 0x2000 1000

Boot modes

Bootloader supports:

- USART1 on pins PA9/PA10, USART2 on pins PA2/PA3, USART3 on pins PC10/PC11
- I2C1 on pins PB6/PB7, I2C2 on pins PB10/PB11, I2C3 on pins PC0/PC1
  - I2C slave address is 0x86
- SPI1 on pins PA4/PA5/PA6/PA7, SPI2 on pins PB12/PB13/PB14/PB15, SPI3 on pins PA15/PC10/PC11/PC12
- USB DFU interface on pins PA11/PA12
  - Bootloader checks if HSE present : USB clock is HSE
  - If no Bootloader checks if LSE present : USB clock is MSI auto-trimmed with LSE

SRAM2 features

- Access through D-code and I-code:
  - Code execution max performance without remap
- **HW parity check** : 4 bit per word
  - Enabled with **SRAM2_PE** in user options bytes
  - **SPF** flag in SYSCFG_CFGR2 when parity check error when reading SRAM2
    - NMI generated
    - Optional Break to Timers (enabled with SPL bit in SYSCFG_CFCR2)
- Optional **retention** in Standby mode with bit **RSS** in PWR_CR3
- **Write protection** with 1 Kbyte granularity:
  - Enabled with **SYSCFG_SWPR** SRAM2 write protection register
- **Read protection** with RDP :
  - Erased when RDP changed from Level 1 to Level 0
- **Software reset** and optional **Hardware reset** when system reset
  - Erased when setting **SRAM2ER** in SYSCFG_SCSR SRAM2 control and status register
  - Erased with system reset with **SRAM2_RST** in user option bytes

CONFIDENTIALITY OBLIGATIONS:

THIS DOCUMENT CONTAINS SENSITIVE INFORMATION.

IT IS CLASSIFIED “MICROCONTROLLERS, MEMORIES & SECURE MCUs (MMS) RESTRICTED AND ITS DISTRIBUTION IS SUBMITTED TO ST/MMS AUTHORIZATION

AT ALL TIMES YOU SHOULD COMPLY WITH THE FOLLOWING SECURITY RULES:

- DO NOT COPY OR REPRODUCE ALL OR PART OF THIS DOCUMENT
- KEEP THIS DOCUMENT LOCKED AWAY
- FURTHER COPIES CAN BE PROVIDED ON A “NEED TO KNOW BASIS”, PLEASE CONTACT YOUR LOCAL ST SALES OFFICE OR DOCUMENT WRITTER.