

1. Description

1.1. Project

Project Name	TouchGFX Simple
Board Name	custom
Generated with:	STM32CubeMX 5.0.0
Date	12/25/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x9
MCU name	STM32F769NIHx
MCU Package	TFBGA216
MCU Pin number	216

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A5	PE1	I/O	FMC_NBL1	
A6	PE0	I/O	FMC_NBL0	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B7	PG15	I/O	FMC_SDNCAS	
B12	PD0	I/O	FMC_D2	
C1	VBAT	Power		
C3	PI4	I/O	FMC_NBL2	
C12	PD1	I/O	FMC_D3	
C13	PI3	I/O	FMC_D27	
C14	PI2	I/O	FMC_D26	
D2	PF0	I/O	FMC_A0	
D3	PI5	I/O	FMC_NBL3	
D4	PI7	I/O	FMC_D29	
D5	PI10	I/O	FMC_D31	
D6	PI6	I/O	FMC_D28	
D10	PJ15 *	I/O	GPIO_Output	DSI_RESET
D13	PH15	I/O	FMC_D23	
D14	PI1	I/O	FMC_D25	
E2	PF1	I/O	FMC_A1	
E4	PI9	I/O	FMC_D30	
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDDSDMMC	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E12	PH13	I/O	FMC_D21	
E13	PH14	I/O	FMC_D22	
E14	PI0	I/O	FMC_D24	
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		

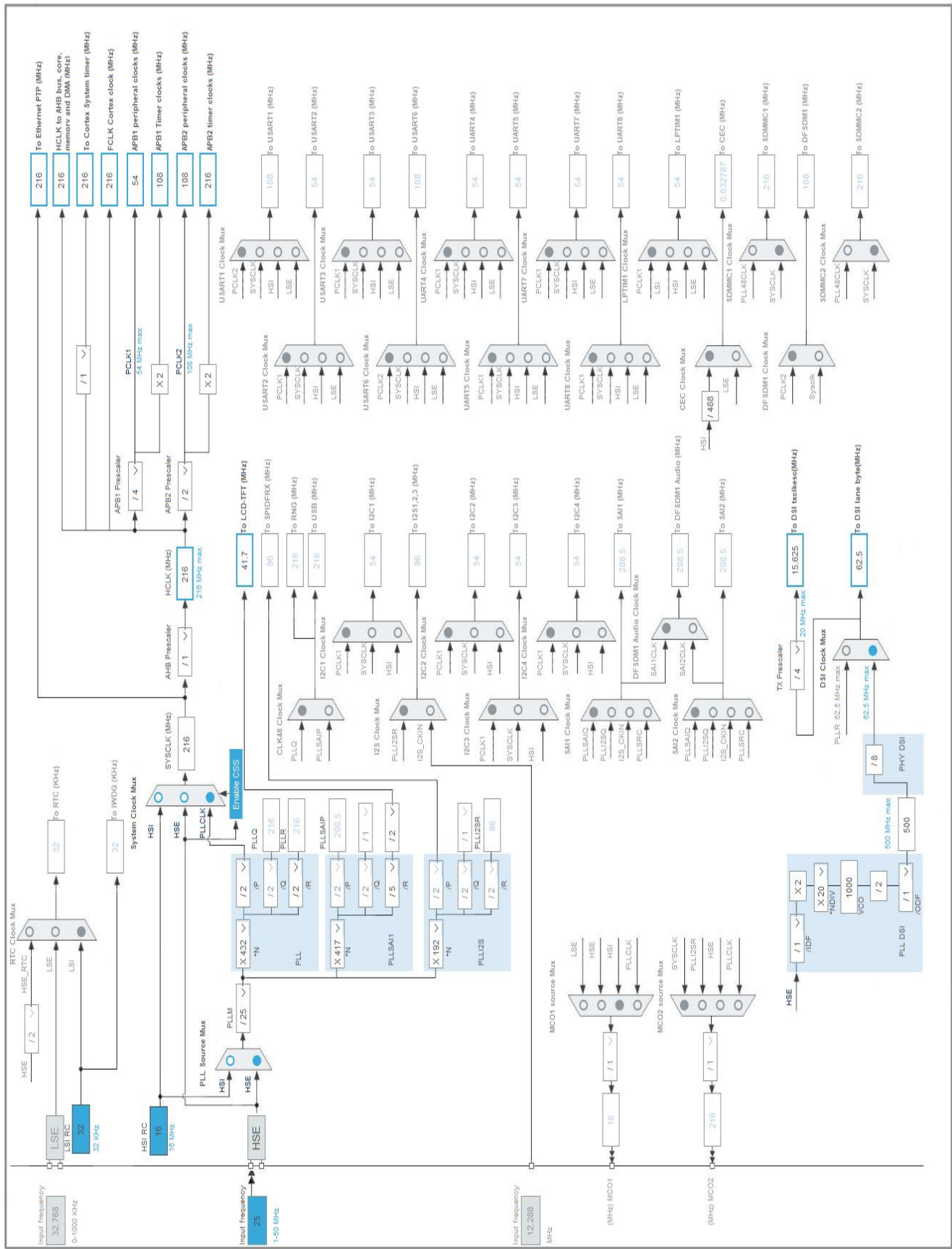
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	DSIHOST_D1P	MonoIO	DSIHOST_D1P	
F13	DSIHOST_D1N	MonoIO	DSIHOST_D1N	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	PF2	I/O	FMC_A2	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	VSSDSI	Power		
G13	VDD12DSI	Power		
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDDDSI	Power		
H12	DSIHOST_CKP	MonoIO	DSIHOST_CKP	
H13	DSIHOST_CKN	MonoIO	DSIHOST_CKN	
H14	PG8	I/O	FMC_SDCLK	
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	
J3	PH5	I/O	FMC_SDNWE	
J4	PH3	I/O	FMC_SDNE0	
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J12	DSIHOST_D0P	MonoIO	DSIHOST_D0P	
J13	DSIHOST_D0N	MonoIO	DSIHOST_D0N	
K3	PF5	I/O	FMC_A5	
K4	PH2	I/O	FMC_SDCKE0	
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	VCAPDSI	Power		
K13	PD15	I/O	FMC_D1	
K15	PD10	I/O	FMC_D15	
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	
L14	PD9	I/O	FMC_D14	
L15	PD8	I/O	FMC_D13	
M1	VSSA	Power		
M6	PF12	I/O	FMC_A6	
M7	PG1	I/O	FMC_A11	
M8	PF15	I/O	FMC_A9	
M15	PH12	I/O	FMC_D20	
N1	VREF-	Power		
N6	PF13	I/O	FMC_A7	
N7	PG0	I/O	FMC_A10	
N9	PE8	I/O	FMC_D5	
N11	PG5	I/O	FMC_BA1	
N12	PG4	I/O	FMC_BA0	
N14	PH9	I/O	FMC_D17	
N15	PH11	I/O	FMC_D19	
P1	VREF+	Power		
P6	PF14	I/O	FMC_A8	
P7	PJ2	I/O	DSIHOST_TE	
P8	PF11	I/O	FMC_SDNRAS	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P11	PE14	I/O	FMC_D11	
P14	PH8	I/O	FMC_D16	
P15	PH10	I/O	FMC_D18	
R1	VDDA	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R8	PE7	I/O	FMC_D4	
R9	PE10	I/O	FMC_D7	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PE13	I/O	FMC_D10	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	TouchGFX_Simple
Project Folder	C:\FelixHu\02_Prj\07_Prj_GUI\02_Prj_TouchGFX\TouchGFX_Simple
Toolchain / IDE	EWARM V8
Firmware Package Name and Version	STM32Cube FW_F7 V1.14.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x9
MCU	STM32F769NIHx
Datasheet	029041 Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. CRC

mode: Activated

7.1.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.2. DMA2D

mode: Activated

7.2.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)

7.3. DSIHOST

DSIHost: Adapted Command Mode with TE Pin

7.3.1. DSI Clocks:

from PLLDSI:

PlIndiv	20
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Pllof	DSI_PLL_OUT_DIV1
Pllidf	DSI_PLL_IN_DIV1
High Speed Clock - PLLDSI Output	500000
Lane Byte Clock	62500
Tx Escape Ckdiv	4
Transmission Escape Clock	15625
Time Out Clock	62500
from PLLR:	
Lane Byte Clock	216000
Transmission Escape Clock	54000
Time Out Clock	216000

7.3.2. Timeout Counters:

Time Out Clock Setting:

Time Out Clock Divider	1
Time Out Clock - from PLLDSI	62500

Contention Error Detection:

High-speed transmission time-out	0
No High-speed transmission time-out	
Low-power reception time-out	0
No Low-power reception time-out	

Peripheral Response:

High-speed read time-out	0
Resulting Timing High-speed read time-out	0
Low-power read time-out	0
Resulting Timing Low-power read time-out	0
High-speed write time-out	0
Resulting Timing High-speed write time-out	0
Low-power write time-out	0
Resulting Timing Low-power write time-out	0
BTA time-out	0
Resulting Timing for BTA time-out	0
High-speed write presp mode	Normal Behavior

7.3.3. Data and Clock Lanes:

Basic Settings:

Number of Lanes	Two Data Lanes *
Automatic Clock Lane Control	Clock Data lane is always provided
Bus Turn Around Request is	Enabled

Flow Control - Configuration:

CRC Reception	Disabled
ECC Reception	Disabled
EoTP Reception is	Disabled
EoTP Transmission is	Disabled
Acknowledge Request after Each Transmission	Enabled *
Tearing Effect Acknowledge Request Enable	Enabled *

Flow Control - Packet Analyzer Configuration:

CRC Error Interrupt	Disable
ECC Errors Interrupt	Disable
EoTP Error Interrupt	Disable
Packet Size Error Interrupt	Disable
Acknowledge Errors Interrupt	Disable
PHY related Errors Interrupt	Disable

7.3.4. PHY Timings:

LP to HS and HS to LP Transitions Timings:

Minimum wait period to request a HS transmission after the Stop state (min est 1 cycle de escape clock)	10 *
Resulting Minimum wait period to request a HS transmission after the Stop state (min est 1 cycle de escape clock)	160

7.3.5. Commands:

APB Interface Error Configuration:

Generic Command Error Interrupt	Disable
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Transmission Mode for Commands::

Generic Short Write Zero Parameter	Low Power Transmission *
Generic Short Write One Parameter	Low Power Transmission *
Generic Short Write Two parameters	Low Power Transmission *
Generic Short Read Zero parameter	Low Power Transmission *
Generic Short Read One parameter	Low Power Transmission *
Generic Short Read Two parameters	Low Power Transmission *
Generic Long Write	Low Power Transmission *
DCS Short Write Zero parameter	Low Power Transmission *
DCS Short Write One parameter	Low Power Transmission *
DCS Short Read Zero parameter	Low Power Transmission *

DCS Long Write	Low Power Transmission *
Maximum Read Packet Size Command	Low Power Transmission *

7.3.6. Display Interface:

Basic Settings:

Display ID	0
Color Coding	RGB888 (24 bits) - DSI mode

Specific Command Mode Settings:

Maximum Command Size	400
The Refresh of the Display Frame Buffer is Triggered	manually by Enabling the LTDC *
Tearing Effect Source	External Source
Polarity of the External Tearing Effect Source	Rising Edge

7.3.7. LTDC Interface:

Clocking:

LTDC Pixel Clock (from Clock tree)	42
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Frame Vertical Timings:

VSA: Vertical Synchronism Active duration (set in LTDC)	2
VBP: Vertical Back-Porch duration (set in LTDC)	1
VFP: Vertical Front-Porch duration (set in LTDC)	1
VACT: Vertical Active duration (set in LTDC)	480

Frame Horizontal Timings:

HSA: Horizontal Synchronism Active duration (set in LTDC)	2
HBP: Horizontal Back-Porch duration (set in LTDC)	1
HACT: Horizontal Active duration (set in LTDC)	400
HLIN: Horizontal Line duration (set in LTDC)	404

Polarity of the Control Signals:

VSYSN Polarity (set in LTDC)	DSI_VSYN_ACTIVE_LOW
HSYSN Polarity (set in LTDC)	DSI_HSYN_ACTIVE_LOW
Data Enable Polarity (set in LTDC)	DSI_DATA_ENABLE_ACTIVE_HIGH

Interface:

The DSI is halting the LTDC synchronously	On a Falling Edge of VSYN
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Interface Error Configuration:

LTDC FIFO Overflow Error Interrupt is	Disabled
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7.4. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 32 bits

Byte enable: 32-bit byte enable

7.4.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	3 memory clock cycles *
Write protection	Disabled
SDRAM common clock	2 HCLK clock cycles *
SDRAM common burst read	Enabled *
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	2 *
Exit self-refresh delay	7 *
Self-refresh time	4 *
SDRAM common row cycle delay	7 *
Write recovery time	3 *
SDRAM common row precharge delay	2 *
Row to column delay	2 *

7.5. LTDC

Display Type: RGB888 (24 bits) - DSI mode

7.5.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	2 *
Horizontal Back Porch	1 *

Active Width	400 *
Horizontal Front Porch	1 *
HSync Width	1
Accumulated Horizontal Back Porch Width	2
Accumulated Active Width	402
Total Width	403

Synchronization for Height:

Vertical Synchronization Height	2 *
Vertical Back Porch	1 *
Active Height	480
Vertical Front Porch	1 *
VSync Height	1
Accumulated Vertical Back Porch Height	2
Accumulated Active Height	482
Total Height	483

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.5.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Number of Layers:

Number of Layers	1 layer *
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Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	400 *
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	480 *

Pixel Parameters:

Layer 0 - Pixel Format	RGB888 *
Blending:	
Layer 0 - Alpha constant for blending	255 *
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant x Pixel Alpha *
Layer 0 - Blending Factor2	Alpha constant x Pixel Alpha *
Frame Buffer:	
Layer 0 - Color Frame Buffer Start Address	0xC0000000 *
Layer 0 - Color Frame Buffer Line Length (Image Width)	400 *
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	480 *

7.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.7. SYS

Debug: Serial Wire

Timebase Source: TIM6

7.8. TIM7

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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7.9. FREERTOS

mode: Enabled

7.9.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Enabled *
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	30720 *

Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled
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Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.9.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled

xTaskGetHandle

Disabled

7.10. GRAPHICS

Graphics Framework: TouchGFX

Display Interface : Display Serial Interface using LTDC-DSIHOST

7.10.1. Parameter Settings:

Stack Name:

Name

TouchGFX

Physical Display Size:

Width

800 *

Height

480 *

Frame Buffer:

LTDC Pixel Format(Set in LTDC)

LTDC_PIXEL_FORMAT_RGB888

Frame Buffer Color Format

RGB888

Color Frame Buffer Depth

24

Color Frame Buffer Start Address(Set in LTDC)

0xc0000000

Buffers Count

Single Buffered

Bitmap Cache Settings:

Bitmap Cache Address

0

Bitmap Cache Size

0

Bitmap Objects Count

0

Instrumentation:

Timer For Instrumentation

Timer 7

LCD Driver:

Use LCD Screen

OTM8009A

OTM8009A Orientation

OTM8009A_ORIENTATION_PORTRAIT

OTM8009A PixelFormat

OTM8009A_FORMAT_RGB888

SDRAM Instances:

SDRAM instance

SDRAM1_BANK1

SDRAM Refresh Count

1835

7.10.2. EA_3_TouchGFX:

External application info:

Name

TouchGFX Designer

Version

V4.10.0

Location:

Executable full name	C:\TouchGFX\4.10.0\designer\ TouchGFXDesigner-4.10.0.exe *
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Inputs:

Physical Display X Size	800
Physical Display Y Size	480

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DSIHOST	DSIHOST_D1P	DSIHOST_D1P	n/a	n/a	n/a	
	DSIHOST_D1N	DSIHOST_D1N	n/a	n/a	n/a	
	DSIHOST_CKP	DSIHOST_CKP	n/a	n/a	n/a	
	DSIHOST_CKN	DSIHOST_CKN	n/a	n/a	n/a	
	DSIHOST_D0P	DSIHOST_D0P	n/a	n/a	n/a	
	DSIHOST_D0N	DSIHOST_D0N	n/a	n/a	n/a	
	PJ2	DSIHOST_TE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI4	FMC_NBL2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI3	FMC_D27	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI2	FMC_D26	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI5	FMC_NBL3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI7	FMC_D29	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI10	FMC_D31	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI6	FMC_D28	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH15	FMC_D23	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI1	FMC_D25	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI9	FMC_D30	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH13	FMC_D21	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH14	FMC_D22	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI0	FMC_D24	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH2	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH12	FMC_D20	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH9	FMC_D17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH11	FMC_D19	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH8	FMC_D16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH10	FMC_D18	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
GPIO	PJ15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DSI_RESET

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
FMC global interrupt	true	5	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
LTDC global interrupt	true	5	0
LTDC global error interrupt	true	5	0
DMA2D global interrupt	true	5	0
DSI global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM7 global interrupt	unused		
FPU global interrupt	unused		

* User modified value

9. Software Pack Report